PATENT APPLICATION

10/550094

JC05 Rec'd PCT/PTO 21 SEP 2005 IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:)	
HANSEN et al.)	Group Art No. TBA
Serial No: TBA)	Examiner: TBA
Filed: Herewith)	Docket No. 006559.00009

For: LIST OUTPUT VITERBI DECODER WITH BLOCKWISE ACS AND TRACEBACK

INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents
U.S. Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 37 C.F.R. §1.56 and in compliance with 37 C.F.R. §1.97, Applicants submit herewith Form PTO-1449 identifying information for consideration by the Examiner. Copies of the cited documents were provided with the International Search Report.

If the Patent and Trademark Office determines that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Date Sept. 21, 2005

Bradley C. Wright Registration No. 38,061

Banner & Witcoff, Ltd. Customer No. 22907

BCW/sdm

JC05 Rec'd PCT/PTO 21 SEP 2005

USPTO Form 1449 Patent and Trademark Office INFORMATION DISCLOSURE CITATION		Attorney Docket No. 006559.00009 TBA								
			Applicant(s): HANSEN et al							
Sheet 1 of 1			Filing Date: September 21, 2005				Group: TBA			
U.S. PATE	ENT DOCUMENTS									
Examiner Initial	Patent No.	Date	Name	Class	Subclass	Subclass Filing Date (if appropriate)				
		·		<u> </u>						
FOREIGN	PATENT DOCUMENT	rs								
Examiner	Document No.	Date	Country	Class	Subclass	Translation				
Initial		16 A 11 1007	Creat Pritain			YES	NO			
	GB 2 305 827 A	16 April 1997	Great Britain			<u> </u>				
							_			
					<u> </u>	<u> </u>	<u> </u>			
OTHER D	OCUMENTS (including	g Author, Title, Date, P	ertinent Pages, etc.)	A algorith	m". TENCO	N '95.				
	CZAJA et al.: "Variable data rate Viterbi decoder with modified LOVA algorithm", TENCON '95, PROCEEEDINGS OF THE IEEE REGION 10 INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND VLSI, Hong Kong, November 6-10, 1995, pages 472-475. XP010160164.									
	BOUTILLON et al.: '	'VLSI architectures for	the MAP Algorithm", II tary 2003, pages 175-185,	EEE TRAN	NSACGION	S ON				
	FETTWEIS et al.: "FOR SIGNAL PROCESSIONAL PROCESSIONAL PROCESSION	eedforward Architectur	res for Parallel Viterbi De IGNAL, IMAGE, AND V	coding", J	OURNAL C	F VLSI FY, vol. 3	3, no. 1 /			
		mailed March 9, 2004								
	SEARCH REPORT,	maned Water 9, 2004				-	-			
		· ·				· · · · · · · · · · · · · · · · · · ·	···			
					 	· · · · · ·				
				1						
EXAMINER				DATE CONSIDERED						
*EXAMINER: In		not citation is in conformance with MP	PEP 609. Draw line through citation if not i	n conformance an	nd not considered. In	nclude copy of	this form with			